What is Claimed is:

1. A memory system comprising:

first and second data memory components for storing data;

one parity memory component for storing parity information;

a first integrated circuit component directly coupled to the first and second data memory components; and

a second integrated circuit component directly coupled to the parity memory component and indirectly coupled to the first and second data memory components through the first integrated circuit, the first integrated circuit being indirectly coupled to the parity memory through the second integrated circuit;

wherein the first integrated circuit is configured to intercommunicate data with a host over a first portion of a system bus, the portion extending between the first integrated circuit and the host, the first and second integrated circuits further including reciprocally-configured logic to inter-communicate such that data communicated between the first integrated circuit and the host is capable of being communicated from the first integrated circuit to the second integrated circuit over a separate bus.

2. The memory system of claim 1, wherein the memory system is a RAID memory system.

3. The memory system of claim 1, wherein the second integrated circuit is configured to intercommunicate data with the host over a second portion of the system bus, wherein the second portion is non-overlapping with the first portion, wherein the second portion extends between the second integrated circuit and the host, the first and second integrated circuits being further configured such that data communicated

between the second integrated circuit and the host is communicated from the second integrated circuit to the first integrated circuit over the separate bus.

4. The memory system of claim 1, further comprising third and fourth data memory components for storing data, and a third integrated circuit component directly coupled to the third and fourth data memory components.

5. The memory system of claim 4, wherein the second integrated circuit component is indirectly coupled to the third and fourth data memory components through the third integrated circuit, and the third integrated circuit is indirectly coupled to the parity memory through the second integrated circuit.

6. The memory system of claim 5, wherein the third integrated circuit is configured to intercommunicate data with the host over a second portion of the system bus, wherein the second portion is non-overlapping with the first portion, wherein the second portion extends between the third integrated circuit and the host, the first, second, and third integrated circuits being further configured such that data communicated between the first integrated circuit and the host is capable of being communicated to the third integrated circuit through the second integrated circuit, such that data communicated between the third integrated circuit and the host is capable of being communicated to the first integrated circuit through the second integrated circuit.

7. The memory system of claim 1, wherein the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus.

8. The memory system of claim 1, wherein the system bus is a point-to-point serial communication bus.

9. A memory system comprising:

a host integrated circuit component;

at least two data memories;

at least one parity memory for storing parity information corresponding to data stored in a corresponding address space of the data memories;

at least two controller integrated circuits, each controller integrated circuit (IC) comprising memory control logic configurable to control communications between the controller IC and data memories directly connected to the controller IC, parity logic configurable to compute parity information for data communicated to or from the data memories, logic configurable to communicate the parity information to or from a companion IC, and logic configurable to communicated data to or from a companion IC.

10. The memory system of claim 9, wherein the memory system is a RAID memory system.

11. The memory system of claim 9, wherein each of the at least two controller integrated circuits further comprises a bus interface for direct coupling to only a portion of a system bus that is coupled to the host for communication therewith.

12. The memory system of claim 11, wherein precisely two controller integrated circuits are configured to implement a RAID 3 memory system, wherein each of the two integrated circuits is configured for direct communication with the host integrated circuit over only a portion of the system bus, wherein a first controller integrated circuit is configured for direct communication with the host integrated circuit over a first portion of the system bus and a second controller integrated circuit is configured for direct communication with the host integrated circuit over a second portion of the system bus.

13. The memory system of claim 9, further including a third controller integrated circuit.

14. The memory system of claim 13, wherein a first and third controller integrated circuit are each configured for direct communication with the host integrated circuit over only a portion of the system bus, wherein a first controller integrated circuit is configured for direct communication with the host integrated circuit over a first portion of the system bus and the third controller integrated circuit is configured for direct communication with the host integrated circuit over a second portion of the system bus.

15. The memory system of claim 14, wherein a second controller integrated circuit includes interfaces for communicating directly with the first and third controller integrated circuits, wherein the second controller integrated circuit is not directly connected to the system but is capable of communicating with the host integrated circuit indirectly through the first and third controller integrated circuits.

16. An integrated circuit component for performing memory control comprising:

host communication logic capable of communicating with a host integrated circuit over only a portion of a system bus;

data memory control logic configurable to control communications with directly connected data memory; and

parity control logic configurable to compute parity information for data stored in associated data memory;

intra-chip communication logic configurable to communicate data and/or parity information with a companion integrated circuit component over a dedicated communication link with the companion integrated circuit;

wherein the data memory control logic, the parity control logic, and the intra-chip communication logic are capable of being configured in one configuration selected from the group consisting of:

a) the data memory control logic is configured to communicate with directly-connected data memory and the parity control logic is configured to communicate parity information indirectly with a parity memory directly connected with a companion integrated circuit via the intra-chip communication logic; and

b) the parity control logic is configured to compute parity information and communicate parity information with a directly-connected parity memory and the data control logic is configured to communicate indirectly with data memory directly connected with a companion integrated circuit via the intra-chip communication logic.